

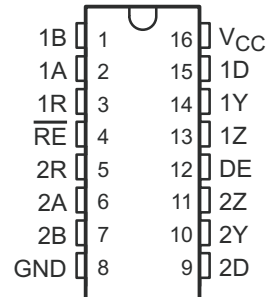
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

Check for Samples: [SN65C1167](#) [SN75C1167](#) [SN65C1168](#) [SN75C1168](#)

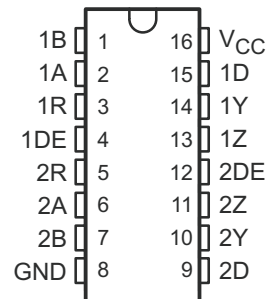
FEATURES

- Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11
- BiCMOS Process Technology
- Low Supply-Current Requirements: 9 mA Max
- Low Pulse Skew
- Receiver Input Impedance . . . 17 k Ω Typ
- Receiver Input Sensitivity . . . ± 200 mV
- Receiver Common-Mode Input Voltage Range of -7 V to 7 V
- Operate From Single 5-V Power Supply
- Glitch-Free Power-Up/Power-Down Protection
- Receiver 3-State Outputs Active-Low Enable for SN65C1167 and SN75C1167 Only
- Improved Replacements for the MC34050 and MC34051

SN65C1167 . . . DB OR NS PACKAGE
SN75C1167 . . . DB, N, OR NS PACKAGE
(TOP VIEW)



SN65C1168 . . . N, NS, OR PW PACKAGE
SN75C1168 . . . DB, N, NS, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION

The SN65C1167, SN75C1167, SN65C1168, and SN75C1168 dual drivers and receivers are integrated circuits designed for balanced transmission lines. The devices meet TIA/EIA-422-B and ITU recommendation V.11.

The SN65C1167 and SN75C1167 combine dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be connected together externally to function as direction control. The SN65C1168 and SN75C1168 drivers have individual active-high enables.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T _A	PACKAGE ^{(1) (2)}		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN75C1167N	SN75C1167N
			SN75C1168N	SN75C1168N
	SOP – NS	Tape and reel	SN75C1167NSR	75C1167
			SN75C1168NSR	75C1168
	SSOP – DB	Tape and reel	SN75C1167DBR	CA1167
			SN75C1168DBR	CA1168
	TSSOP – PW	Tube	SN75C1168PW	CA1168
		Tape and reel	SN75C1168PWR	
–40°C to 85°C	PDIP – N	Tube	SN65C1168N	SN65C1168N
			SN65C1167NSR	65C1167
	SOP – NS	Tape and reel	SN65C1168NSR	65C1168
			SN65C1167DBR	CB1167
	TSSOP – PW	Tube	SN65C1168PW	CB1168
		Tape and reel	SN65C1168PWR	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/sc/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTION TABLES

Each Driver⁽¹⁾

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

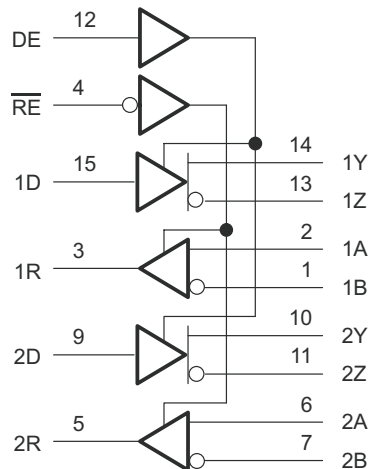
Each Receiver⁽¹⁾

DIFFERENTIAL INPUTS A – B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z
Open	L	H

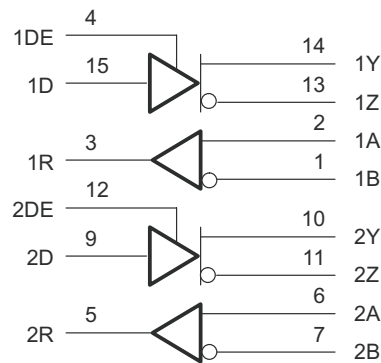
(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)

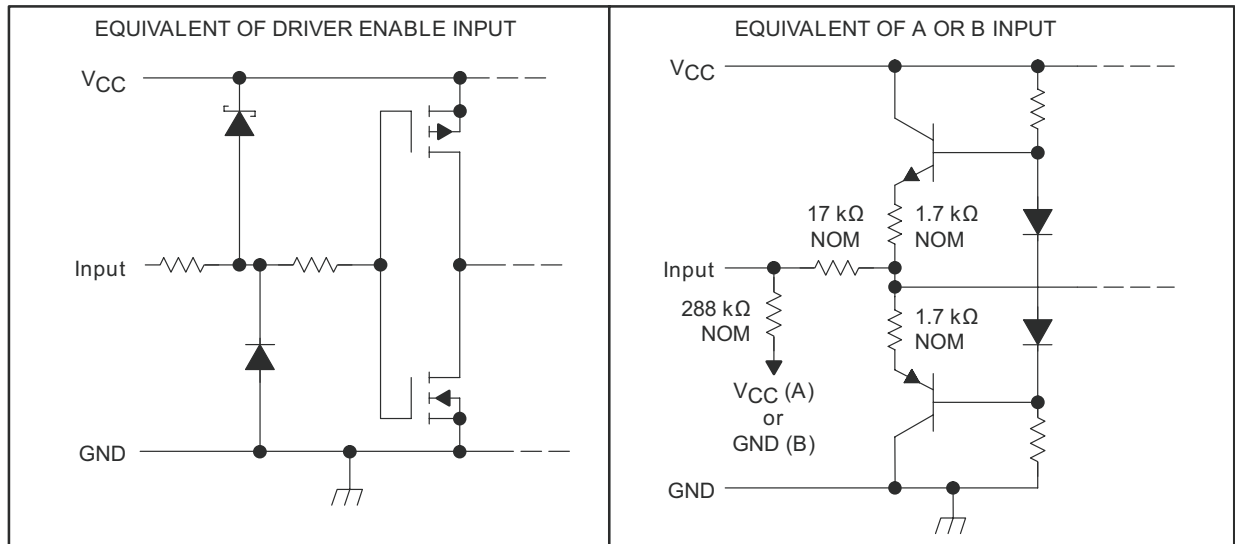
SN65C1167/SN75C1167



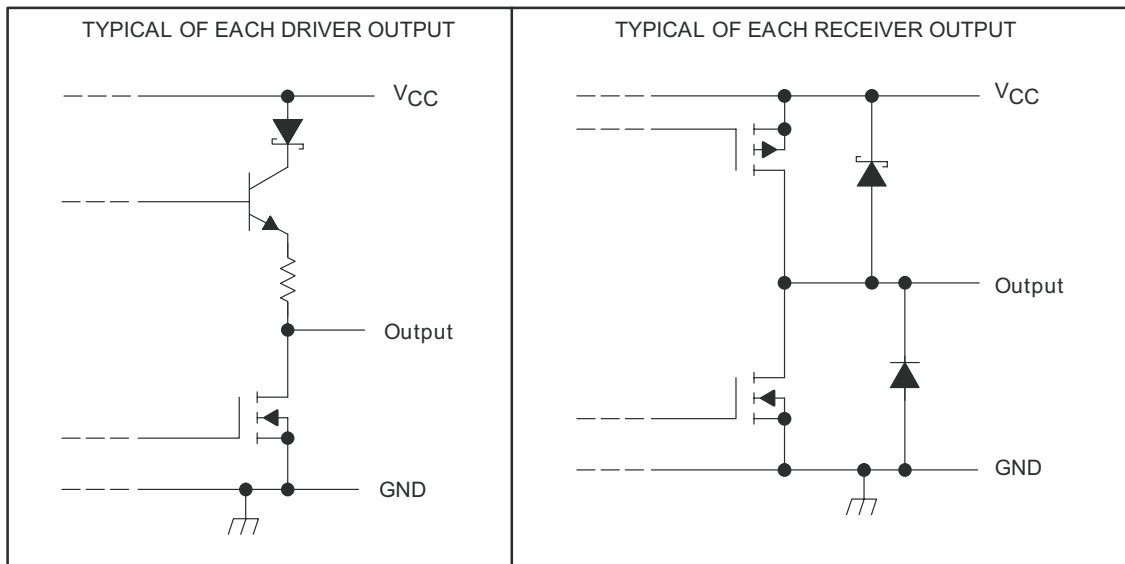
SN65C1168, SN75C1168



SCHEMATIC OF INPUTS



SCHEMATIC OF OUTPUTS



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range ⁽²⁾	-0.5	7	V	
V _I	Input voltage range	Driver	-0.5	V _{CC} + 0.5	V
		A or B, Receiver	-11	14	
V _{ID}	Differential input voltage range ⁽³⁾	Receiver	-14	14	V
V _O	Output voltage range	Driver	-0.5	7	V
I _{IK} or I _{OK}	Clamp current range	Driver		±20	mA
I _O	Output current range	Driver		±150	mA
		Receiver		±25	
I _{CC}	Supply current		200	mA	
	GND current		-200	mA	
T _J	Operating virtual junction temperature		150	°C	
θ _{JA}	Package thermal impedance ^{(4) (5)}	DB package		82	°C/W
		N package		67	
		NS package		64	
		PW package		108	
T _{stg}	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages values except differential input voltage are with respect to the network GND.
- (3) Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
- (4) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{IC}	Common-mode input voltage ⁽¹⁾	Receiver		±7	V
V _{ID}	Differential input voltage	Receiver		±7	V
V _{IH}	High-level input voltage	Except A, B	2		V
V _{IL}	Low-level input voltage	Except A, B		0.8	V
I _{OH}	High-level output current	Receiver		-6	mA
		Driver		-20	
I _{OL}	Low-level output current	Receiver		6	mA
		Driver		20	
T _A	Operating free-air temperature	SN75C1167, SN75C1168	0	70	°C
		SN65C1167, SN65C1168	-40	85	

- (1) Refer to TIA/EIA-422-B for exact conditions.

DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT	
V _{IK}	Input clamp voltage	I _I = -18 mA				-1.5	V	
V _{OH}	High-level output voltage	V _{IH} = 2 V,	V _{IL} = 0.8 V, I _{OH} = -20 mA	2.4	3.4		V	
V _{OL}	Low-level output voltage	V _{IH} = 2 V,	V _{IL} = 0.8 V, I _{OL} = 20 mA		0.2	0.4	V	
V _{OD1}	Differential output voltage	I _O = 0 mA		2		6	V	
V _{OD2}	Differential output voltage ⁽¹⁾	R _L = 100 Ω, See Figure 1		2	3.1		V	
Δ V _{OD}	Change in magnitude of differential output voltage					±0.4	V	
V _{OC}	Common-mode output voltage						±3	V
Δ V _{OC}	Change in magnitude of common-mode output voltage						±0.4	V
I _{O(OFF)}	Output current with power off	V _{CC} = 0 V	V _O = 6 V V _O = -0.25 V			100 -100	μA	
I _{OZ}	High-impedance-state output current	V _O = 2.5 V V _O = 5 V				20 -20	μA	
I _{IH}	High-level input current	V _I = V _{CC} or V _{IH}				1	μA	
I _{IL}	Low-level input current	V _I = GND or V _{IL}				-1	μA	
I _{OS}	Short-circuit output current ⁽³⁾	V _O = V _{CC} or GND,		-30		-150	mA	
I _{CC}	Supply current (total package) ⁽⁴⁾	No load, Enabled	V _I = V _{CC} or GND V _I = 2.4 or 0.5 V		4 5	6 3	mA	
C _i	Input capacitance				6		pF	

(1) Refer to TIA/EIA-422-B for exact conditions.

(2) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

(4) This parameter is measured per input, while the other inputs are at V_{CC} or GND.

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PHL}	Propagation delay time, high- to low-level output	R1 = R2 = 50 Ω, C1 = C2 = C3 = 40 pF, See Figure 2	R3 = 500 Ω, S1 is open,		7	12	ns
t _{PLH}	Propagation delay time, low- to high-level output				7	12	ns
t _{sk(p)}	Pulse skew				0.5	4	ns
t _r	Rise time	R1 = R2 = 50 Ω, C1 = C2 = C3 = 40 pF, See Figure 3	R3 = 500 Ω, S1 is open,		5	10	ns
t _f	Fall time				5	10	ns
t _{PZH}	Output enable time to high level	R1 = R2 = 50 Ω, C1 = C2 = C3 = 40 pF, See Figure 4	R3 = 500 Ω, S1 is closed,		10	19	ns
t _{PZL}	Output enable time to low level				10	19	ns
t _{PHZ}	Output disable time from low level	R1 = R2 = 50 Ω, C1 = C2 = C3 = 40 pF, See Figure 4	R3 = 500 Ω, S1 is closed,		7	16	ns
t _{PLZ}	Output disable time from high level				7	16	ns

(1) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

RECEIVER SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input					0.2	V
V_{IT-}	Negative-going input threshold voltage, differential input			-0.2 ⁽²⁾			V
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK}	Input clamp voltage, \overline{RE}	SN75C1167	$I_I = -18$ mA			-1.5	V
V_{OH}	High-level output voltage		$V_{ID} = 200$ mV, $I_{OH} = -6$ mA	3.8	4.2		V
V_{OL}	Low-level output voltage		$V_{ID} = -200$ mV, $I_{OL} = 6$ mA		0.1	0.3	V
I_{OZ}	High-impedance-state output current	SN75C1167	$V_O = V_{CC}$ or GND		± 0.5	± 5	μ A
I_I	Line input current		Other input at 0 V	$V_I = 10$ V		1.5	mA
				$V_I = -10$ V		-2.5	
I_I	Enable input current, \overline{RE}	SN75C1167	$V_I = V_{CC}$ or GND			± 1	μ A
r_i	Input resistance		$V_{IC} = -7$ V to 7 V, Other input at 0 V	4	17		k Ω
I_{CC}	Supply current (total package)		No load, Enabled	$V_I = V_{CC}$ or GND		4	6
				$V_{IH} = 2.4$ V or 0.5 V ⁽³⁾		5	9

(1) All typical values are at $V_{CC} = 5$ V and $T_A = 25^\circ$ C.

(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) Refer to TIA/EIA-422-B for exact conditions.

Switching Characteristics

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 5		9	17	27	ns
t_{PHL}	Propagation delay time, high- to low-level output			9	17	27	ns
t_{TLH}	Transition time, low- to high-level output	$V_{IC} = 0$ V, See Figure 5			4	9	ns
t_{THL}	Transition time, high- to low-level output				4	9	ns
t_{PZH}	Output enable time to high level	$R_L = 1$ kW, See Figure 6			13	22	ns
t_{PZL}	Output enable time to low level				13	22	ns
t_{PHZ}	Output disable time from high level				13	22	ns
t_{PLZ}	Output disable time from low level				13	22	ns

(1) Measured per input while the other inputs are at V_{CC} or GND

(2) All typical values are at $V_{CC} = 5$ V and $T_A = 25^\circ$ C.

PARAMETER MEASUREMENT INFORMATION

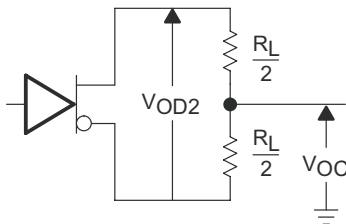


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

- A. C1, C2, and C3 include probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r = t_f \leq 6$ ns.

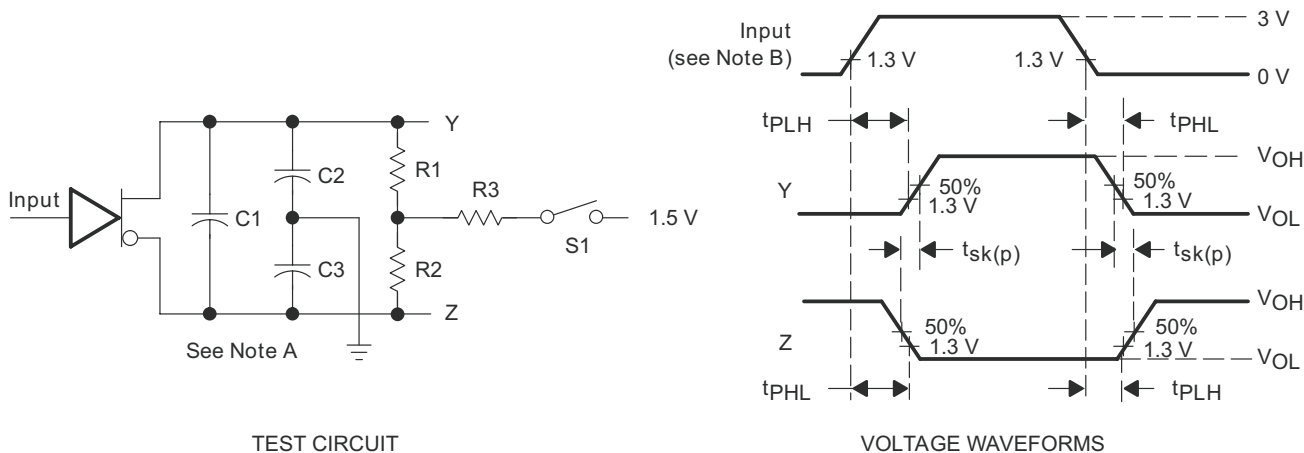


Figure 2. Driver Test Circuit and Voltage Waveforms

- C. C1, C2, and C3 include probe and jig capacitance.
- D. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r = t_f \leq 6$ ns.

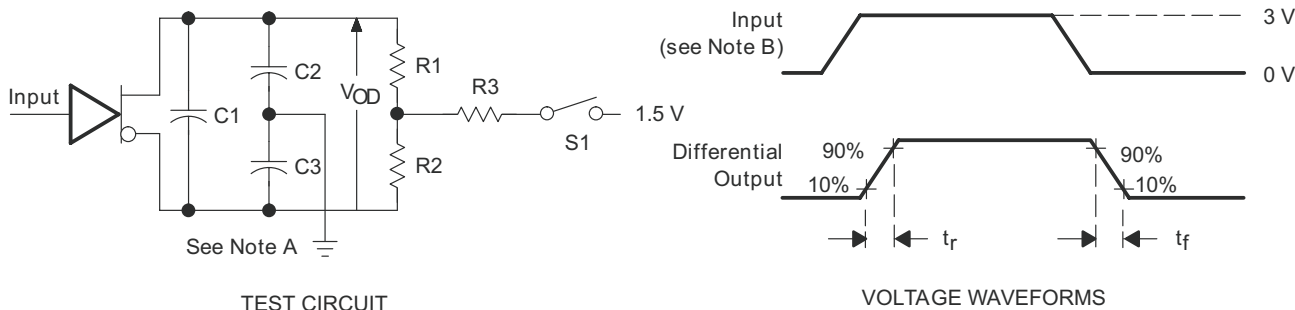


Figure 3. Driver Test Circuit and Voltage Waveforms

- E. C1, C2, and C3 include probe and jig capacitance.
- F. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r = t_f \leq 6$ ns.

PARAMETER MEASUREMENT INFORMATION (continued)

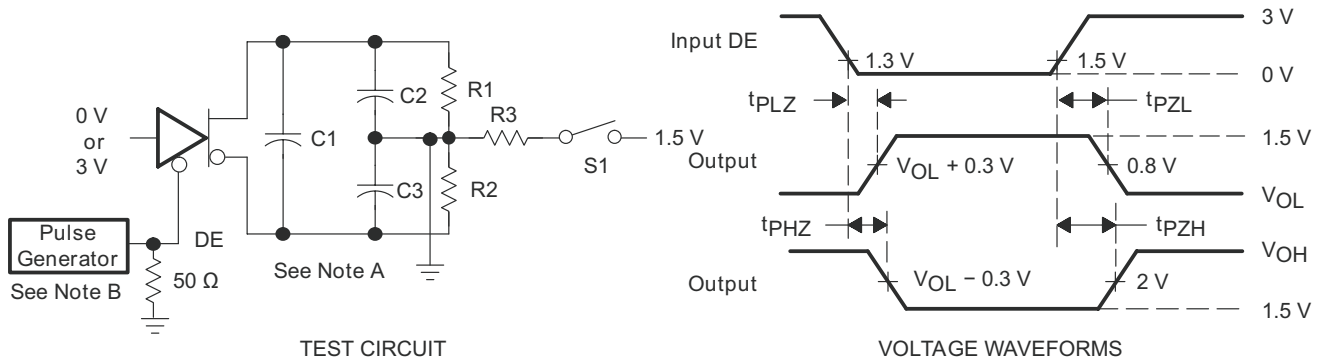


Figure 4. Driver Test Circuit and Voltage Waveforms

- G. C_L includes probe and jig capacitance.
- H. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r = t_f \leq 6$ ns.

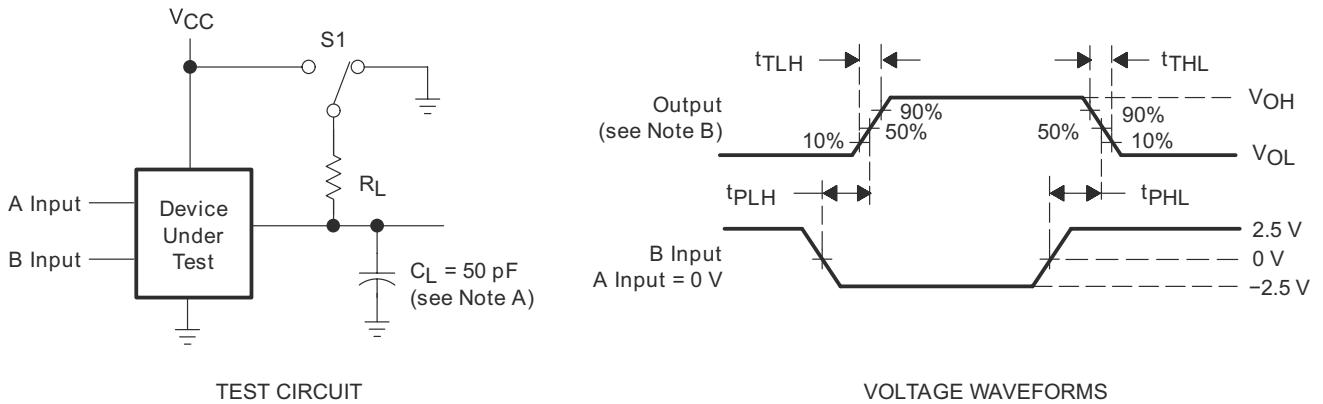


Figure 5. Receiver Test Circuit and Voltage Waveforms

- I. C_L includes probe and jig capacitance.
- J. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r = t_f \leq 6$ ns.

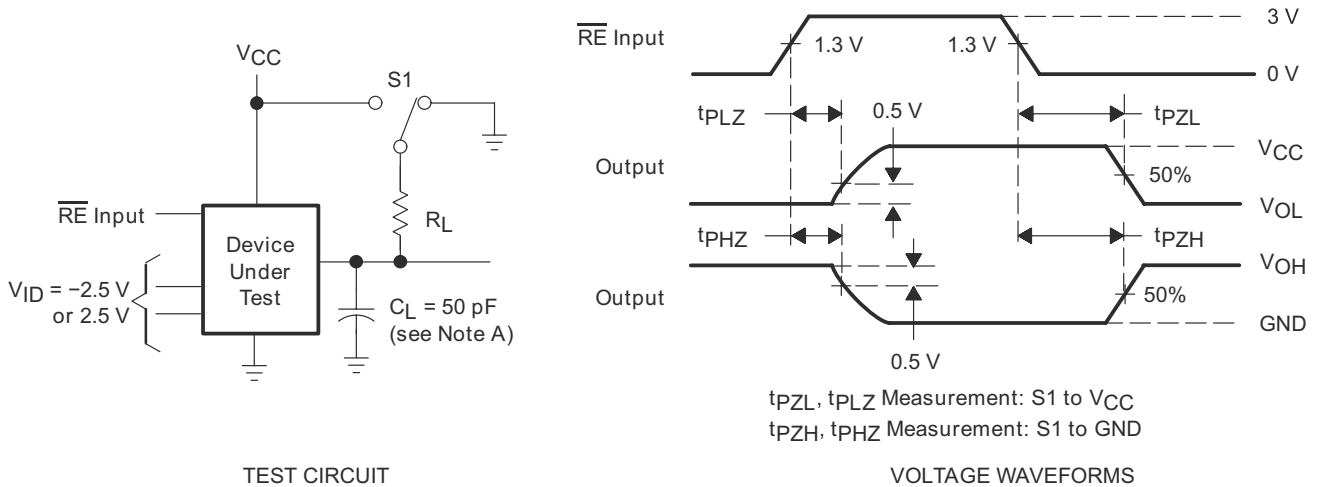


Figure 6. Receiver Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C1167NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167	Samples
SN65C1167NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167	Samples
SN65C1168N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN65C1168N	Samples
SN65C1168NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168	Samples
SN65C1168NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168	Samples
SN65C1168PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN65C1168PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN65C1168PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168	Samples
SN75C1167DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1167	Samples
SN75C1167N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75C1167N	Samples
SN75C1167NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1167	Samples
SN75C1167NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1167	Samples
SN75C1168DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75C1168N	Samples
SN75C1168NE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75C1168N	Samples
SN75C1168NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1168	Samples
SN75C1168NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75C1168	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75C1168PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples
SN75C1168PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	CA1168	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C1167NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C1168NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C1168PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75C1167DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75C1168DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75C1168PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C1167NSR	SO	NS	16	2000	367.0	367.0	38.0
SN65C1168NSR	SO	NS	16	2000	367.0	367.0	38.0
SN65C1168PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN75C1167DBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN75C1168DBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN75C1168PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

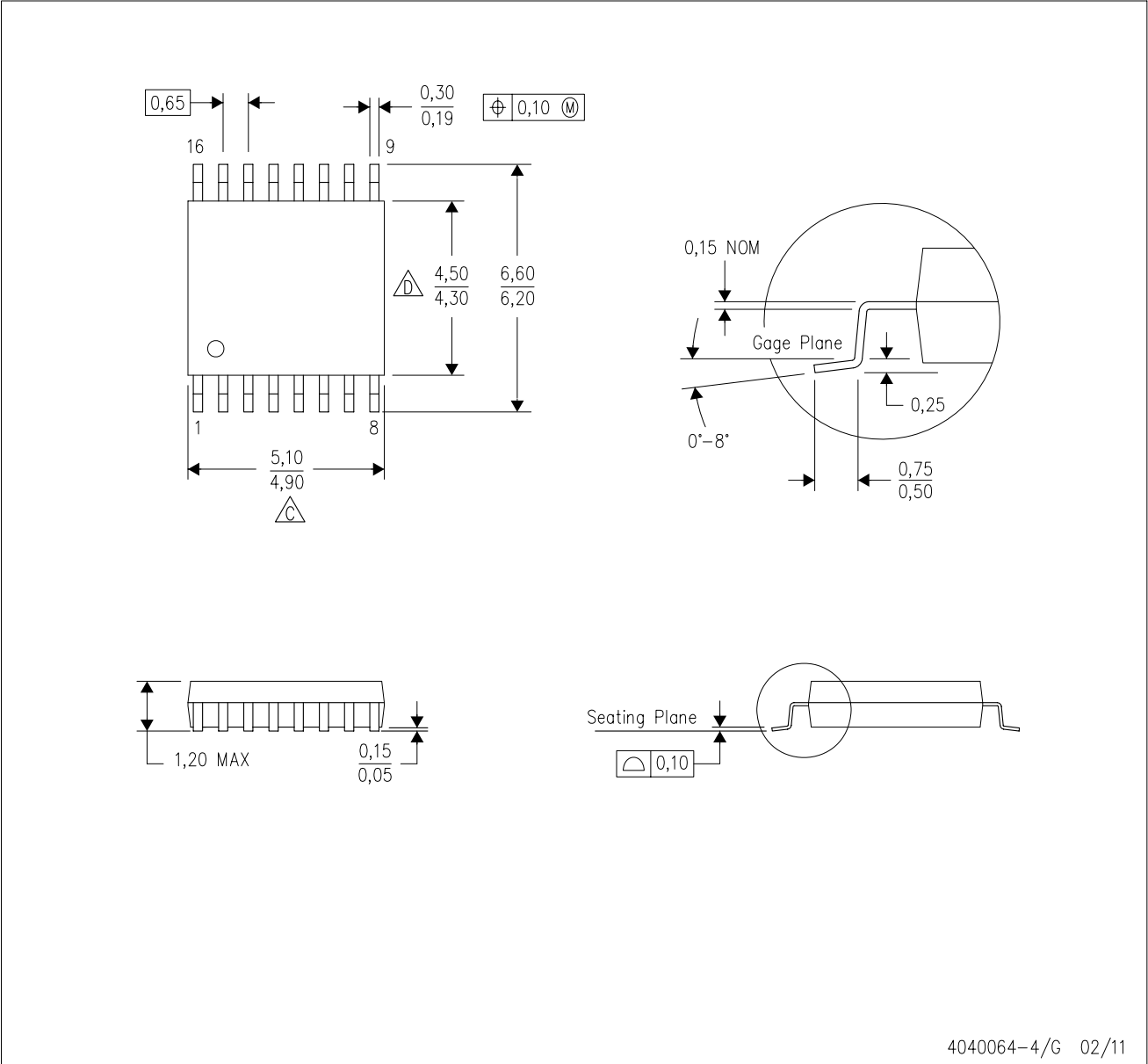


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Texas Instruments:](#)

[SN75C1167DBR](#) [SN75C1167N](#) [SN75C1167NSR](#) [SN75C1167NSRG4](#) [SN75C1167DBRG4](#)